REMARKS

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

Various editorial amendments have been made to the specification and abstract. No new matter has been added. A substitute specification and abstract along with a marked-up copy of the substitute specification and abstract are submitted herewith.

The specification was objected to for the informalities set forth on page 2 of the Office Action. Also, claims 1-10 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for the reasons set forth on pages 3 and 4 of the Office Action. It is requested that these objections and rejections be withdrawn in view of the current amendments and the following remarks.

The Examiner requests further explanation regarding whether the phase control circuit 12 shifts the output of the comparison circuit 11 rather than the phase of the clock of the present reference signal. The phase control circuit does not shift the output of the comparison circuit, but rather shifts the phase state of the present reference signal based on the output of the comparison circuit. That is, the phase control circuit shifts the phase state of the present reference signal based on the result of the comparison between the previous reference signal and the present reference signal. When the phase control circuit 12 receives the comparison result between the present reference signal and the previous reference signal outputted from the comparison circuit 11, the phase control circuit 12 counts the clock number by an internal circuit until the phase state of the present reference signal matches the phase state of the previous reference signal, and performs the counting until the output of the XOR circuit 26 finally becomes "0." When the output of the XOR circuit becomes "0," the selector control circuit 13 controls the selector 14 so as to select one clock among the clocks outputted from the delay cells 2-5 as a synchronous clock that is finally outputted.

Thus, the phase control circuit does not shift the phase of the present reference signal per se. Rather, as shown in Fig. 20, the phase states of the present reference signal and the previous reference signal are detected by the comparison circuit 11, and the phase control circuit 12 performs a count-up or count-down control based on the detected

information, thereby shifting the phase state of the present reference signal. Further, comparison of this phase shifted signal and the previous reference signal is performed.

The Examiner also requested an explanation of "(1-N/N) clock." This is the result of a typographical error, and has been changed throughout the application to the correct "(N-1)/N clock." The (N-1)/N clock is obtained by subtracting 1/N clock period from the clock. For example, in certain embodiments disclosed in the application, the phase control circuit performs a phase-shift control at a "3/4" clock rate internal. The "3/4 clock" is the (N-1)/N clock, where N is 4.

The Examiner also requested an explanation of "counts the number of clocks in units of 1/M lines (M: integer not less than 2)" and "the phase of the clock of the present reference signal can be controlled in units of 1/M lines." The phrase 1/M lines means that one line period is divided into M parts equally. "M" denotes the number of clocks per one line. The phrase "counts the number of clocks in units of 1/M lines (M: integer not less than 2)" means that the phase control circuit counts the number of clocks by a unit of 1/M lines and performs a phase-control on the basis of the count value. For example, when one line is divided into three parts equally, the circuit counts the number of clocks every 1/3 line. The phrase "the phase of the clock of the present reference signal can be controlled in units of 1/M lines" means that the phase control circuit counts the number of clocks every 1/M line and interprets a phase state of the present reference signal on the basis of the count value so as to perform a phase control.

Regarding claims 2 and 3 (new claims 12 and 13), the term "clock" is used throughout the application, as is common practice in the art, to refer to one clock period. Thus, the phase control circuit counts the number of clock periods, or fractions thereof, corresponding to the phase difference between the present reference signal and the previous reference signal.

Regarding claim 4 (new claim 14), the (1+N)/N clock is obtained by adding a clock period and 1/N clock period together. For example, in embodiments discussed in the specification, the phase control circuit performs a phase shift control at a 5/4 clock rate interval. The "5/4 clock" is the (1+N)/N clock, where N is 4.

Regarding claim 5 (new claim 15), as discussed above, the (N-1)/N clock is obtained by subtracting 1/N clock period from the clock. For example, in certain

embodiments disclosed in the application, the phase control circuit performs a phase-shift control at a "3/4" clock rate internal. The "3/4 clock" is the (N-1)/N clock, where N is 4.

Regarding claim 8 (new claim 18), the phrase "clock by clock" means that the phase control circuit counts the number of clock periods by a unit of a clock period so as to detect the phase difference between the present reference signal and the previous reference signal.

Regarding claim 9 (new claims 19), please see the discussion above regarding 1/M lines.

Regarding claim 10, the phrase "line by line" means that the phase control circuit counts the number of clocks by a unit of a line so as to detect the phase difference between the present reference signal and the previous reference signal.

Claims 1-3 were rejected under 35 U.S.C. § 102(b) as being anticipated by Jung (US 6,342,796). This rejection is traversed and is inapplicable to new claims 11-13.

New claim 11 recites a reference signal phase detection circuit for detecting a phase state of a present reference signal based on phase differences between clocks outputted from a plurality of delay cells and the present reference signal, and detecting a phase state of a previous reference signal based on phase differences between the clocks outputted from the delay cells and the previous reference signal, a comparison circuit for comparing the phase state of the present reference signal and the phase state of the previous reference signal, and a phase control circuit for shifting the phase state of the present reference signal to make it coincide with the phase state of the previous reference signal.

Jung does not disclose or suggest such features. While Jung discloses delay lines, the apparatus of Jung does not detect a phase state of a present reference signal based on phase differences between clocks outputted from the delay lines and a present reference signal, and detect a phase state of a previous reference signal based on phase differences between clocks outputted from the delay lines and the previous reference signal. Moreover, while Jung discloses a phase comparator and a shift controller, the phase comparator of Jung does not compare a phase state of a present reference signal and a phase state of a previous reference signal, and the shift controller does not shift the phase state of the present reference signal to make it coincide with the phase state of the

previous reference signal. Accordingly, claims 11-13 are not anticipated by Jung.

In view of the above, it is submitted that claims 11-20 are allowable over the prior art of record and that the present application is in condition for allowance.

Respectfully submitted,

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